AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Previously Presented) An active matrix substrate, comprising:

first bus lines and second bus lines arranged to form a matrix;

switching devices provided near respective intersections of the first bus lines and the second bus lines; and

pixel electrodes electrically connected to the first bus lines and the second bus lines through the switching devices, wherein:

at least one of the first bus lines has a first capacitance formed thereon,

the first bus lines, except for the at least one first bus line with a first capacitance, are connected to first bus lines on another active matrix substrate, and

the first capacitance is formed by arranging (i) a first bus line not connected to first bus lines on another active matrix substrate and (ii) a line other than the second bus lines to cross each other.

2. (Original) The active matrix substrate as set forth in claim 1, wherein

the at least one first bus line with a first capacitance is connected to a line connected to no pixel electrode on the other active matrix substrate.

3. (Original) The active matrix substrate as set forth in claim 1, wherein

each of those first bus lines which have no first capacitance formed thereon has a second capacitance formed thereon which is less than the first capacitance.

4. (Original) The active matrix substrate as set forth in claim 1, wherein

the first bus lines are connected to a source driver, and the second bus lines are connected to a gate driver.

5. (Original) The active matrix substrate as set forth in claim 1, wherein

the first bus lines are connected to a gate driver, and the second bus lines are connected to a source driver.

6. (Previously Presented) A display, comprising an active matrix substrate including:

first bus lines and second bus lines arranged to form a matrix;

switching devices provided near respective intersections of the first bus lines and the second bus lines; and

pixel electrodes electrically connected to the first bus lines and the second bus lines through the switching devices, wherein:

at least one of the first bus lines has a first capacitance formed thereon,

the first bus lines, except for the at least one first bus line with a first capacitance, are connected to first bus lines on another active matrix substrate, and

the first capacitance is formed by arranging (i) a first bus line not connected to first bus lines on another active matrix substrate and (ii) a line other than the second bus lines to cross each other.

7. (Previously Presented) A display, comprising display panels each including an active matrix substrate including:

first bus lines and second bus lines arranged to form a matrix;

switching devices provided near respective intersections of the first bus lines and the second bus lines; and

pixel electrodes electrically connected to the first bus lines and the second bus lines through the switching devices, wherein:

at least one of the first bus lines has a first capacitance formed thereon,

the first bus lines, except for the at least one first bus line with a first capacitance, are shared for use among the active matrix substrates in the display panels, and

the first capacitance is formed by arranging (i) a first bus line that is on an active matrix substrate and that is not shared for use with another active matrix substrate and (ii) a line other than the second bus lines to cross each other.

8. (Original) The display as set forth in claim 7, wherein

the first bus lines shared among the display panels each have a second capacitance formed thereon which is less than the first capacitance.

9. (Original) The display as set forth in claim 7, further comprising a source driver and a gate driver for applying a signal voltage to the first bus lines and the second bus lines, wherein

the first bus lines are connected to the source driver, and the second bus lines are connected to the gate driver.

10. (Original) The display as set forth in claim 7, further comprising a source driver and a gate driver for applying a signal voltage to the first bus lines and the second bus lines, wherein

the first bus lines are connected to the gate driver, and the second bus lines are connected to the source driver.

11. (Original) The display as set forth in claim 7, wherein

one of the display panels is designated as a main panel, and the display panels, except for the main panel, are designated as sub-panels having less display pixels than the main panel.

12. (Previously Presented) A display, comprising display panels each including an active matrix substrate including:

first bus lines and second bus lines arranged to form a matrix;

switching devices provided near respective intersections of the first bus lines and the second bus lines; and

pixel electrodes electrically connected to the first bus lines and the second bus lines through the switching devices, wherein:

the first bus lines are shared for use among the display panels,

in at least one of the display panels, at least one of the first bus lines is connected to none of the pixel electrodes on the active matrix substrate,

the at least one first bus line connected to none of the pixel electrodes has a first capacitance formed thereon, and

the first capacitance is formed by arranging (i) a first bus line not connected to the pixel electrodes and (ii) a line other than the second bus lines to cross each other.

13. (Original) The display as set forth in claim 12, wherein

each of those first bus lines which have no first capacitance formed thereon has a second capacitance formed thereon which is less than the first capacitance.

14. (Original) The display as set forth in claim 12, further comprising a source driver and a gate driver for applying a signal voltage to the first bus lines and the second bus lines, wherein

the first bus lines are connected to the source driver, and the second bus lines are connected to the gate driver.

15. (Original) The display as set forth in claim 12, further comprising a source driver and a gate driver for applying a signal voltage to the first bus lines and the second bus lines, wherein

the first bus lines are connected to the gate driver, and the second bus lines are connected to the source driver.

16. (Original) The display as set forth in claim 12, wherein

one of the display panels is designated as a main panel, and the display panels, except for the main panel, are designated as sub-panels having less display pixels than the main panel.

17. (Previously Presented) The active matrix substrate as set forth in claim 1, wherein

an amount of the first capacitance is such that there is substantially no difference in signal delay on each first bus line of the active matrix substrate that is connected to a first bus line on the other active matrix substrate and signal delay on the at least one first bus line with a first capacitance.

18. (Previously presented) The display as set forth in claim 6, wherein

an amount of the first capacitance is such that there is substantially no difference in signal delay on each first bus line of the active matrix substrate that is connected to a first bus line on the other active matrix substrate and signal delay on the at least one first bus line with a first capacitance.

19. (Previously presented) The display as set forth in claim 7, wherein

an amount of the first capacitance is such that there is substantially no difference in signal delay on each first bus line that is shared for use among the active matrix substrates in the display panels and signal delay on the at least one first bus line with a first capacitance.

20. (Previously presented) The display as set forth in claim 12, wherein

an amount of the first capacitance is such that there is substantially no difference in signal delay on each first bus line that is shared for use among the display panels and signal delay on the at least one the first bus line with a first capacitance.

21. (New) The active matrix substrate as set forth in claim 1, wherein the active matrix substrate has a display area and the first capacitance is formed outside the display area.

22. (New) The display as set forth in claim 6, wherein the active matrix substrate has a display area and the first capacitance is formed outside the display area.

23. (New) The display as set forth in claim 7, wherein the active matrix substrate has a display area and the first capacitance is formed outside the display area.

24. (New) The display as set forth in claim 12, wherein the active matrix substrate has a display area and the first capacitance is formed outside the display area.

25. (New) The active matrix substrate (or display) as set forth in claim 1, wherein said line other than the second bus lines is a signal line for a dummy pixel.

26. (New) The display as set forth in claim 6, wherein said line other than the second bus lines is a signal line for a dummy pixel.

27. (New) The display as set forth in claim 7, wherein said line other than the second bus lines is a signal line for a dummy pixel.

28. (New) The display as set forth in claim 12, wherein said line other than the second bus lines is a signal line for a dummy pixel.